Serial No.: 09/539,206

REMARKS

Claims 1-3 are presently under consideration in the application. Claims 4-8 have been withdrawn from consideration as a result of a previous election. Applicants have amended the title of the invention as requested by the Examiner. Favorable reconsideration of the application is respectfully requested.

I. ALLOWABLE SUBJECT MATTER

Applicants note with appreciation the indicated allowability of claims 2 and 3. These claims will be in condition for allowance upon being amended to independent form.

II. REJECTION OF CLAIM 1 UNDER 35 USC §102(b)

Claim 1 remains rejected under 35 USC §102(b) based on *Johnson et al.* Applicants respectfully request withdrawal of the rejection for at least the following reasons.

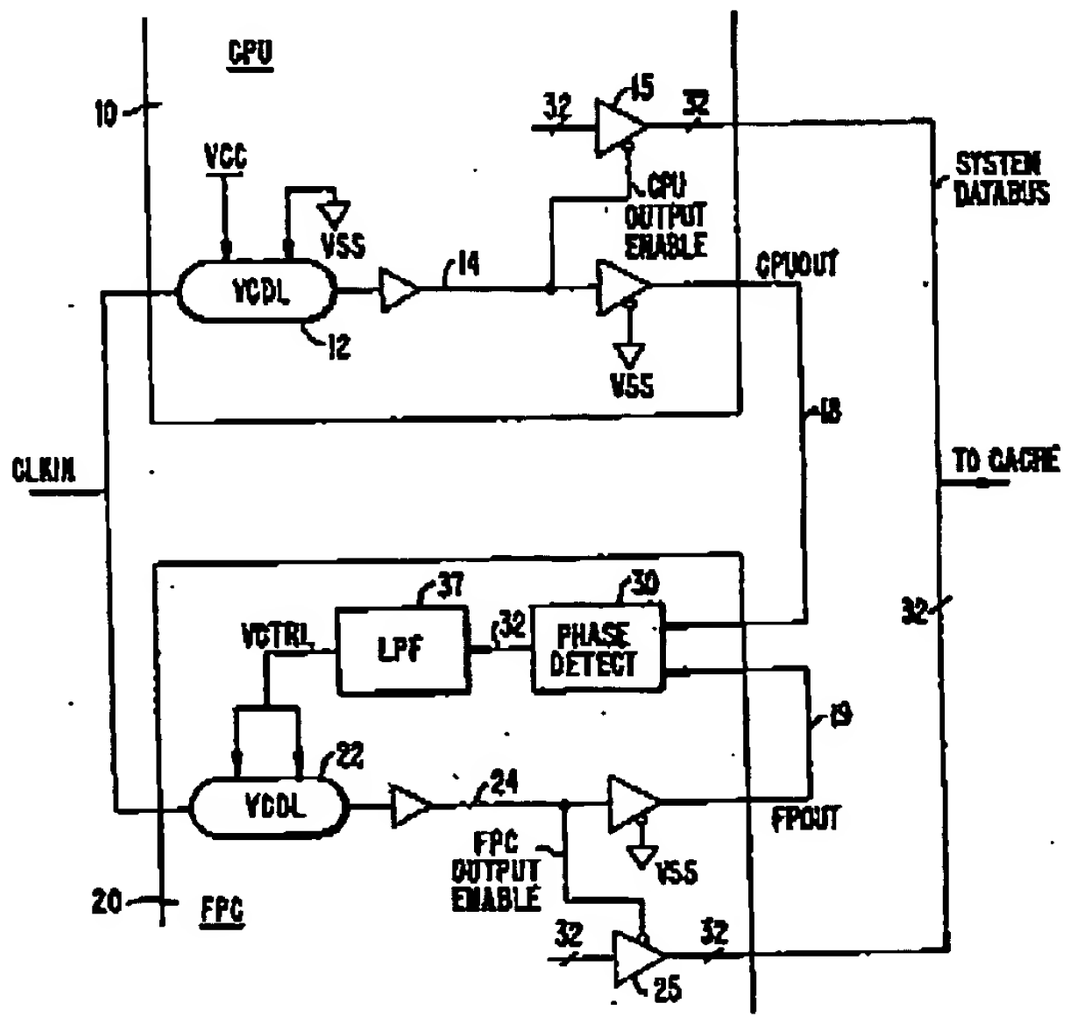

Fig. 1 of Johnson et al.

Serial No.: 09/539,206

Regarding Claim 1, Applicants previously argued how the Examiner associates element 12 in *Johnson et al.* (see Fig. 1, reproduced above) as corresponding to the "first delay portion driven by a first driving voltage" as recited in claim 1. Applicants acknowledged that element 12 in *Johnson et al.* is in fact a voltage-controlled delay line. However, applicants pointed out that the voltage-controlled delay line 12 delays the clock signal supplied thereto by a *fixed* time interval. (See e.g., Col. 2, lns. 32-35). Specifically, *Johnson et al.* teaches that the control voltage inputs for the voltage-controlled delay line 12 are tied to fixed voltages Vcc and Vss. (See, e.g., Fig. 1 and Col. 4, lns. 56-62). Thus, the delay interval will be fixed.

In response, the Examiner indicates that contrary to applicants' arguments *Johnson et al.* does provide a clock signal that is delayed by an adjustable interval through a voltage-control delay line. In supporting such conclusion, however, the Examiner now cites portions of the text in *Johnson et al.* relating to the fixed voltage-control delay line 12 and the adjustable voltage-control delay line 22. In other words, the Examiner relies on the characteristics of the different voltage-control delay lines 12 and 22 in concluding that the single first delay portion recited in claim 1 is anticipated.

Even more significantly, applicants previously argued how *Johnson et al.* does not teach or suggest a voltage supplying portion which supplies the first driving voltage to the first delay portion in such a manner that "the first delay time is substantially equal to a clock period of the clock signal" received by the first delay portion, as recited in claim 1. *Johnson et al.* teaches a circuit having a clock signal at 16.7 MHz, thus rendering a clock period of approximately 60 nanoseconds (ns). (Col. 2, lns. 51-55). Fig. 5 of *Johnson et al.* illustrates the operation of the voltage-controlled delay line 12. (Col. 4, ln. 56 - Col. 5, ln. 9). As is shown in Fig. 5, the maximum contemplated delay period for the delay line 12 is approximately 18 ns. The maximum contemplated delay of the voltage-controlled delay line 12 of 18 ns is far short of the clock period (i.e., 60 ns) as taught in *Johnson et al.* Accordingly, *Johnson et al.* does not teach or suggest the first delay time is substantially equal to a clock period of the clock signal as recited in claim 1 of the present application.

In response, the Examiner indicates "applicant also argues 'this is far short of a clock period (i.e., 60 ns) as required in claim 1 of the present application.' Applicants' argument is not persuasive since it is not drawn to the claimed subject matter." (O.A., p. 4).

For the Examiner to state that the argument is not drawn to the claimed subject matter suggests that the Examiner feels the applicants were arguing that claim 1 does not recite a clock period equal to 60 ns. Applicants believe the Examiner may have misunderstood the argument and does not appreciate that the exemplary numbers (i.e., 18 ns and 60 ns) were provided in order to illustrate that the delay provided by the delay line 12 in *Johnson et al.* is not "substantially equal to a clock period of the clock signal" as is recited in claim 1. Nor, for that matter, does *Johnson et al.* teach or suggest that the delay line 22 provides such a delay time.

In other words, even if the present invention and *Johnson et al.* teach producing a delay time in a signal from a delay portion by changing a driving voltage, the present invention adjusts (by means of a delay circuit 212 as shown in Figs. 4A and 4B, for example) that delay time of the signal, e.g., the value of the delay amount of the delay circuit 212 becomes substantially equal to the clock period of the clock signal. *Johnson et al.* does not teach or suggest such an arrangement as recited in claim 1.

Johnson et al. discloses an arrangement in which the delaying amount of VCDL22 is equal to the delaying amount of VCDL12 which is a replica, the output signal of VCD122 being the same period of a clock signal. However, there is no mechanism to provide that a delaying time, i.e., an absolute value of delaying amount is substantially equal to a clock period of the clock signal as recited in claim 1.

Accordingly, applicants again respectfully submit that *Johnson et al.* does not teach or suggest a first delay portion driven in such a manner that the first delay time is substantially equal to a clock period of the clock signal as recited in claim 1. Withdrawal of the rejection of claim 1 is therefore respectfully requested.

III. CONCLUSION

Accordingly, all claims 1-3 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should a petition for an extension of time be necessary for the timely reply to the outstanding Office Action (or if such a petition has been made and an additional extension is necessary), petition is hereby made and the Commissioner is authorized to charge any fees (including additional claim fees) to Deposit Account No. 18-0988.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

Mark D. Saralino
Reg. No. 34,243

DATE: May 20, 2005

The Keith Building
1621 Euclid Avenue
Nineteenth Floor
Cleveland, Ohio 44115
(216) 621-1113
B:\GEN\YAMA\Yama705\yamap705.aaf.wpd